WHAT IS CLAIMED IS:

1. A manufacturing method of a semiconductor integrated circuit device having an information transfer MISFET and a capacitor connected in series to said information transfer MISFET, the manufacturing method comprising the steps of:

(a) forming a gate insulating film and a gate electrode on a semiconductor substrate;

(b) forming a source and drain regions in the semiconductor substrate on both sides of said gate electrode;

(c) forming an insulating film on said gate electrode and said source and drain regions;

(d) depositing a first shielding film on said insulating film;

(e) depositing a first conductive film, a capacitive insulating film made of a ferroelectric material, and a second conductive film on said first shielding film patterning the deposited films exclusive of said first shielding film; and thereby forming on said first shielding film, a capacitor which is constituted by a lower electrode composed of the first conductive film, a capacitive insulating film, and an upper electrode composed of the second conductive film; and

(f) forming a second shielding film composed of an insulating film so as to cover sidewalls of said upper electrode and said capacitor.

2. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein the step of forming said insulating film includes a step of annealing in a hydrogen atmosphere.

3. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said insulating film is formed by a plasma CVD method.

4. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said insulating film is a silicon oxide film and is formed by performing a heat treatment to an SOG film.

5. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said first and second shielding films and said capacitive insulating film are insulating films each made of a lead compound.

6. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said first and second shielding films and said capacitive insulating film are PZT films.

7. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said capacitor is formed on said information transfer MISFET through said insulating film

said insulating film is formed on a source and drain regions of said information transfer MISFET,

said second shielding film is formed on the source and drain regions of said information transfer MISFET, and

a plug is formed so that a conductive film is embedded in a first contact hole formed by removing said insulating film and said second shielding film disposed on the source or drain region of said information transfer MISFET, the plug being connected to said lower electrode.

8. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said capacitor is formed on said information transfer MISFET through said insulating film

said insulating film is formed on a source and drain regions of said information transfer MISFET,

said second shielding film is formed on the source and drain regions of said information transfer MISFET,

a plug is formed so that a conductive film is embedded in a first contact hole formed by removing said insulating film and said second shielding film disposed on one of the source and drain regions of said information transfer MISFET, the plug being connected to said lower electrode, and

a second contact hole is formed in said insulating film and said second shielding film disposed on the other of the source and drain regions of said information transfer MISFET, the second contact hole being connected to a wiring.

9. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said first shielding film is composed of an insulating film.

10. The manufacturing method of a semiconductor integrated circuit device according to claim 1, further comprising a step of:

depositing, on said information transfer MISFET and said capacitor, a first insulating film, a barrier layer made of a high-diaelectric-constant material or ferroelectric material, and a second insulating film in this order, and thereby forming an interlayer insulating film.

11. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said first and second shielding films and said capacitive insulating film are insulating films each made of a lead compound, and

each lead composition ratio of said shielding films is higher than that of said capacitive insulating film.

12. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said capacitive insulating film is a first PZT film ($Pb_{x1}(Zr_{y1}Ti_{z1})O_3$) and each of said shielding films is a second PZT film ($Pb_{x2}(Zr_{y2}Ti_{z2})O_3$)where $x2 > x1$.